



Reg. No. :

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Question Paper Code : X20478

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Third Semester

Electrical and Electronics Engineering
EE 6301 – DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering Instrumentation
and Control Engineering)
(Regulations 2013)

(Also Common to PTEE 6301 – Digital Logic Circuits for B.E. (Part – Time)
Electrical and Electronics Engineering Third Semester – (Regulations 2014))

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions

PART – A

(10×2=20 Marks)

1. Construct OR gate and AND gate using NAND gates.
2. Convert the following Excess-3 numbers into decimal numbers :
 - a) 1011
 - b) 1001 0011 0111.
3. What is a K-map ?
4. Compare decoder and demultiplexer.
5. Convert T Flip Flop to D Flip Flop.
6. State the rules for state assignment.
7. What are the two types of asynchronous sequential circuits ?
8. State the difference between PROM, PLA and PAL.
9. Give the syntax for package declaration and package body in VHDL.
10. Write the VHDL code for a 2×1 multiplexer using behavioural modeling.



PART – B

(5×13=65 Marks)

11. a) Explain in detail about error detecting and error correcting code. **(13)**
 (OR)
- b) Write short notes on following :
- i) RTL **(3)**
 - ii) DTL **(3)**
 - iii) TTL and **(4)**
 - iv) ECL. **(3)**
12. a) i) Reduce the following function using K-map. **(7)**
 $f(A, B, C, D) = \pi M(0, 2, 3, 8, 9, 12, 13, 15)$
- ii) Design a full adder using two half-adders and an OR gate. **(6)**
 (OR)
- b) i) Design a BCD to Excess 3 code converter. **(7)**
 ii) Implement the following Boolean function using 8 : 1 Mux : **(6)**
 $F(A, B, C, D) = \Sigma m(0, 1, 3, 4, 8, 9, 15).$
13. a) Design a sequence detector that produces an output '1' whenever the non-overlapping sequence 101101 is detected. **(13)**
 (OR)
- b) i) Explain the realization of JK flip flop from T flip flop. **(7)**
 ii) Write short notes on SIPO and draw the output waveforms. **(6)**
14. a) i) What are Static-0 and Static-1 hazards ? Explain the removal of hazards using hazard covers in K-map. **(7)**
 ii) Explain cycles and races in asynchronous sequential circuits. **(6)**
 (OR)
- b) i) What are transition table and flow table ? Give suitable examples. **(5)**
 ii) Implement the following function using PLA and PAL : **(8)**
 $f(x, y, z) = \Sigma m(0, 1, 3, 5, 7).$
15. a) Design a 3-bit magnitude comparator and write the VHDL code to realize it using structural modeling. **(13)**
 (OR)
- b) Design a 4×4 array multiplier and write the VHDL code to realize it using structural modeling. **(13)**



PART – C

(1×15=15 Marks)

16. a) Assume that there is a parking area in a shop whose capacity is 10. No more than 10 cars are allowed inside the parking area and the gate is closed as soon as the capacity is reached. There is a gate sensor to detect the entry of car which is to be synchronized with the clock pulse. Design and implement a suitable counter using JK flip flops. Also, determine the number of flip flops to be used if the capacity is increased to 50. **(15)**

(OR)

- b) Design a 4 bit code converter which converts given binary code into a code in which the adjacent number differs by only 1 by the preceding number. Also, develop VHDL coding for the above mentioned code converter. **(15)**
